MOTOROLA Semiconductors

SN 74S241 ← sostituire con

MC3448A

LS 243

BIDIRECTIONAL INSTRUMENTATION BUS (GP-IB) TRANSCEIVER

This bidirectional bus transeiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1975, often referred to as GP-IB). The required bus termination is internally provided.

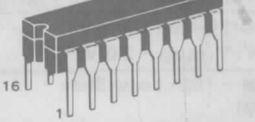
Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by its corresending Send/Receive input with the disabled output of the pair forced to a high impedance state. An additional option allows the driver outputs to be operated in an open collector or active pull-up configuration. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

- Four Independent Driver/Receiver Pairs
- Three-State Outputs
- High Impedance Inputs
- Receiver Hysteresis — 600 mV (Typ)
- Fast Propagation Times — 15-20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output Option
- Power Up/Power Down Protection (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power Is Removed From Device
- Required Termination Characteristics Provided

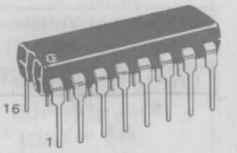
QUAD THREE-STATE BUS TRANSCEIVER WITH TERMINATION NETWORKS

SILICON MONOLITHIC INTEGRATED CIRCUIT

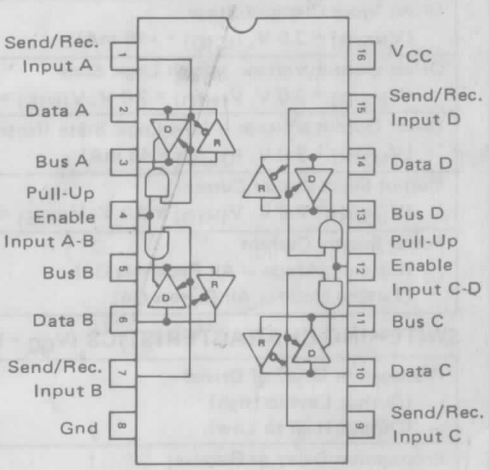
SILVERSTAR LTD S.p.A.
Via del Gracchi, 20
20146 MILANO - Telefono 4996



L SUFFIX
CERAMIC PACKAGE
CASE 620

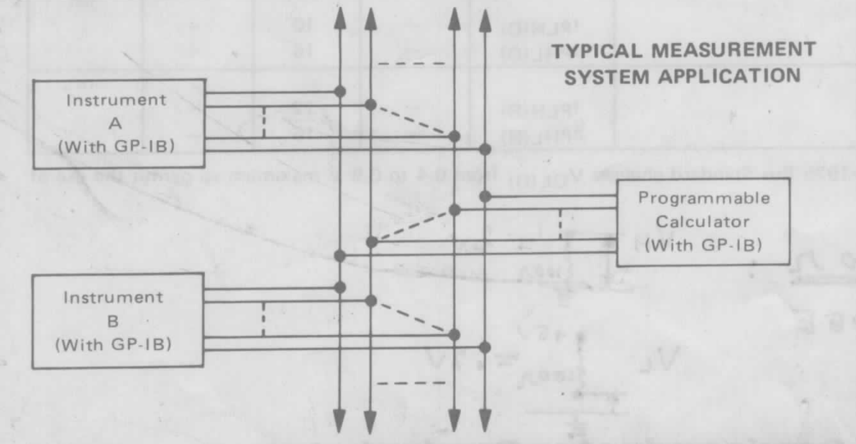


P SUFFIX
PLASTIC PACKAGE
CASE 648



MAXIMUM RATINGS ($T_A = 25^oC$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	T_J	150	^oC
Operating Ambient Temperature Range	T_A	0 to +70	^oC
Storage Temperature Range	T_{stg}	-65 to +150	^oC


Instrument A (With GP-IB)
Instrument B (With GP-IB)
Programmable Calculator (With GP-IB)
16 Lines Total

TYPICAL MEASUREMENT SYSTEM APPLICATION

TRUTH TABLE

Send/Rec.	Enable	Info. Flow	Comments
0	X	Bus → Data	—
1	1	Data → Bus	Active Pull-Up
1	0	Data → Bus	Open Col.

X = Don't Care

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ELECTRICAL CHARACTERISTICS

(Unless otherwise noted 4.75 V ⩽ V_{CC} ⩽ 5.25 V and 0 ⩽ T_A ⩽ 70°C; typical values are at T_A = 25°C, V_{CC} = 5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
Bus Voltage					V
(Bus Pin Open)($V_{I(S/R)}$ = 0.8 V)	$V_{(BUS)}$	2.75	—	3.7	
($I_{(BUS)}$ = −12 mA)	$V_{IC(BUS)}$	—	—	−1.5	
Bus Current	$I_{(BUS)}$				mA
(5.0 V ⩽ $V_{(BUS)}$ ⩽ 5.5 V)		0.7	—	2.5	
($V_{(BUS)}$ = 0.8 V)		−1.5	—	−3.2	
(V_{CC} = 0 V, 0 V ⩽ $V_{(BUS)}$ ⩽ 2.75 V)		—	—	−0.04	
Receiver Input Hysteresis ($V_{I(S/R)}$ = 0.8 V)	—	400	600	—	mV
Receiver Input Threshold					V
($V_{I(S/R)}$ = 0.8 V, Low to High)	$V_{ILH(R)}$	—	1.6	1.8	
($V_{I(S/R)}$ = 0.8 V, High to Low)	$V_{IHL(R)}$	0.8	1.0	—	
Receiver Output Voltage — High Logic State ($V_{I(S/R)}$ = 0.8 V, $I_{OH(R)}$ = −800 μA, $V_{(BUS)}$ = 2.0 V)	$V_{OH(R)}$	2.7	—	—	V
Receiver Output Voltage — Low Logic State ($V_{I(S/R)}$ = 0.8 V, $I_{OL(R)}$ = 16 mA, $V_{(BUS)}$ = 0.8 V)	$V_{OL(R)}$	—	—	0.5	V
Receiver Output Short Circuit Current ($V_{I(S/R)}$ = 0.8 V, $V_{(BUS)}$ = 2.0 V)	$I_{OS(R)}$	−15	—	−75	mA
Driver Input Voltage — High Logic State ($V_{I(S/R)}$ = 2.0 V)	$V_{IH(D)}$	2.0	—	—	V
Driver Input Voltage — Low Logic State ($V_{I(S/R)}$ = 2.0 V)	$V_{IL(D)}$	—	—	0.8	V
Driver Input Current — Data Pins ($V_{I(S/R)}$ = $V_{I(E)}$ = 2.0 V)					μA
(0.5 ⩽ $V_{I(D)}$ ⩽ 2.7 V)	$I_{I(D)}$	−200	—	40	
($V_{I(D)}$ = 5.5 V)	$I_{IB(D)}$	—	—	200	
Input Current — Send/Receive					μA
(0.5 ⩽ $V_{I(S/R)}$ ⩽ 2.7 V)	$I_{I(S/R)}$	−100	—	20	
($V_{I(S/R)}$ = 5.5 V)	$I_{IB(S/R)}$	—	—	100	
Input Current — Enable					μA
(0.5 ⩽ $V_{I(E)}$ ⩽ 2.7 V)	$I_{I(E)}$	−200	—	20	
($V_{I(E)}$ = 5.5 V)	$I_{IB(E)}$	—	—	100	
Driver Input Clamp Voltage ($V_{I(S/R)}$ = 2.0 V, $I_{IC(D)}$ = −18 mA)	$V_{IC(D)}$	—	—	−1.5	V
Driver Output Voltage — High Logic State ($V_{I(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V, $V_{IH(E)}$ = 2.0 V, I_{OH} = −5.2 mA)	$V_{OH(D)}$	2.5	—	—	V
Driver Output Voltage — Low Logic State (Note 1) ($V_{I(S/R)}$ = 2.0 V, $I_{OL(D)}$ = 48 mA)	$V_{OL(D)}$	—	—	0.5	V
Output Short Circuit Current ($V_{I(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V, $V_{IH(E)}$ = 2.0 V)	$I_{OS(D)}$	−30	—	−120	mA
Power Supply Current					mA
(Listening Mode — All Receivers On)	I_{CCL}	—	63	85	
(Talking Mode — All Drivers On)	I_{CCH}	—	106	125	

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Propagation Delay of Driver					ns
(Output Low to High)	$t_{PLH(D)}$	—	10	—	
(Output High to Low)	$t_{PHL(D)}$	—	16	—	
Propagation Delay of Receiver					ns
(Output Low to High)	$t_{PLH(R)}$	—	22	—	
(Output High to Low)	$t_{PHL(R)}$	—	16	—	

NOTE 1. A pending modification of the IEEE 488-1975 Bus Standard changes $V_{OL(D)}$ from 0.4 to 0.5 V maximum to permit the use of Schottky technology.

Lato "Data" : su 100 Ω :

DA QUESTO LATO LE LINEE

// NON SONO O.C. //

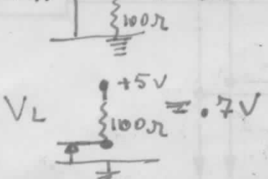
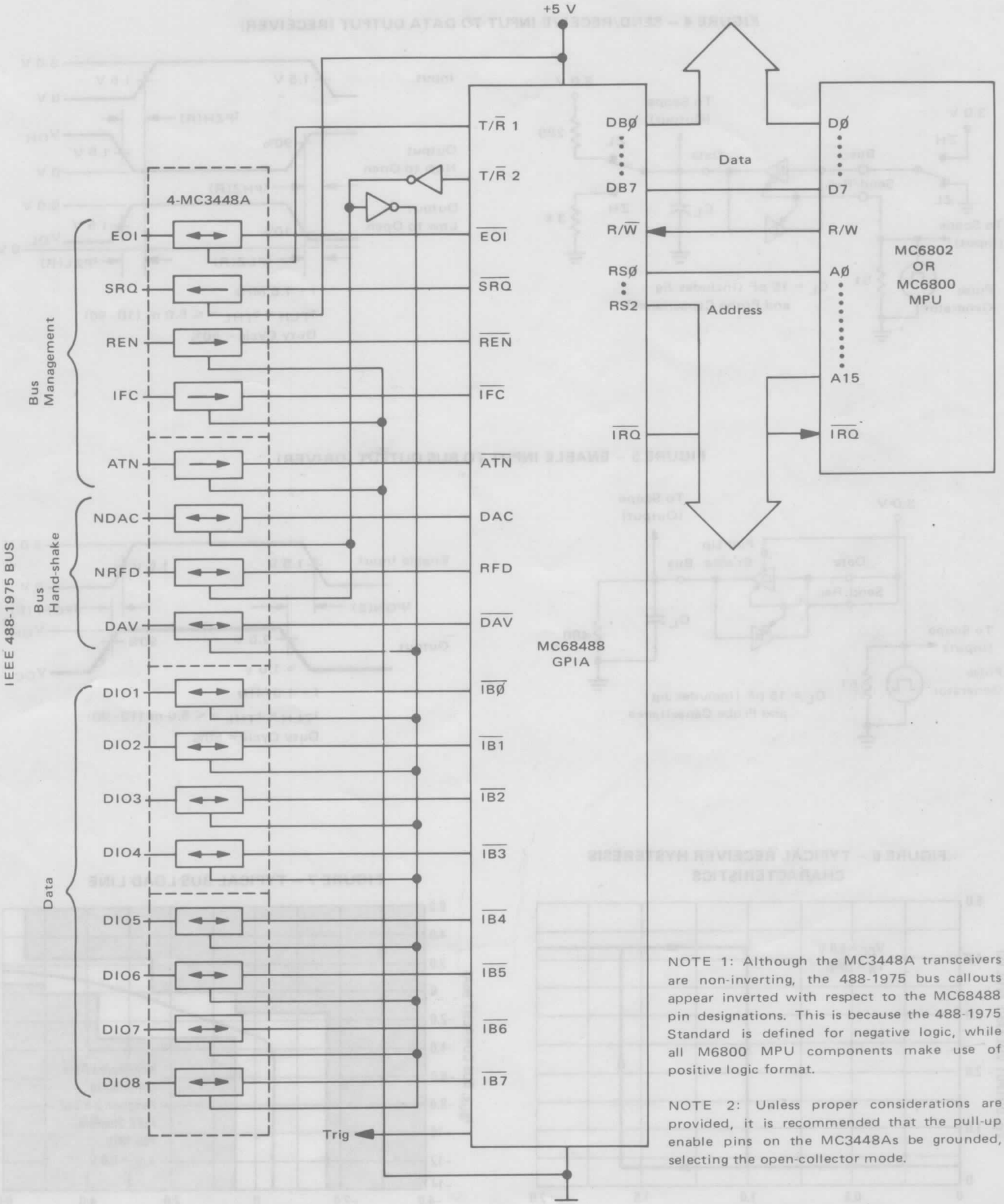


FIGURE 8 – SIMPLE SYSTEM CONFIGURATION



NOTE 1: Although the MC3448A transceivers are non-inverting, the 488-1975 bus callouts appear inverted with respect to the MC68488 pin designations. This is because the 488-1975 Standard is defined for negative logic, while all M6800 MPU components make use of positive logic format.

NOTE 2: Unless proper considerations are provided, it is recommended that the pull-up enable pins on the MC3448As be grounded, selecting the open-collector mode.

FIGURE 4 – SEND/RECEIVE INPUT TO DATA OUTPUT (RECEIVER)

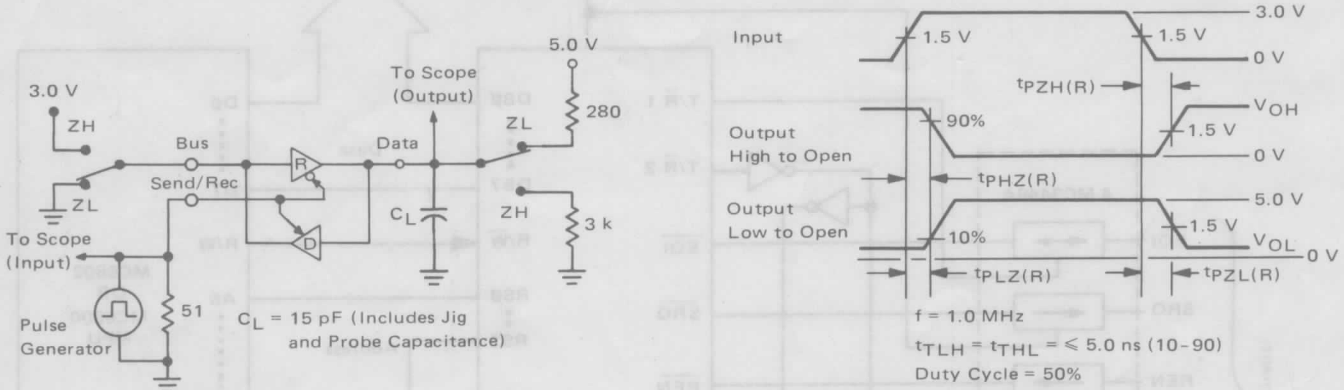


FIGURE 5 – ENABLE INPUT TO BUS OUTPUT (DRIVER)

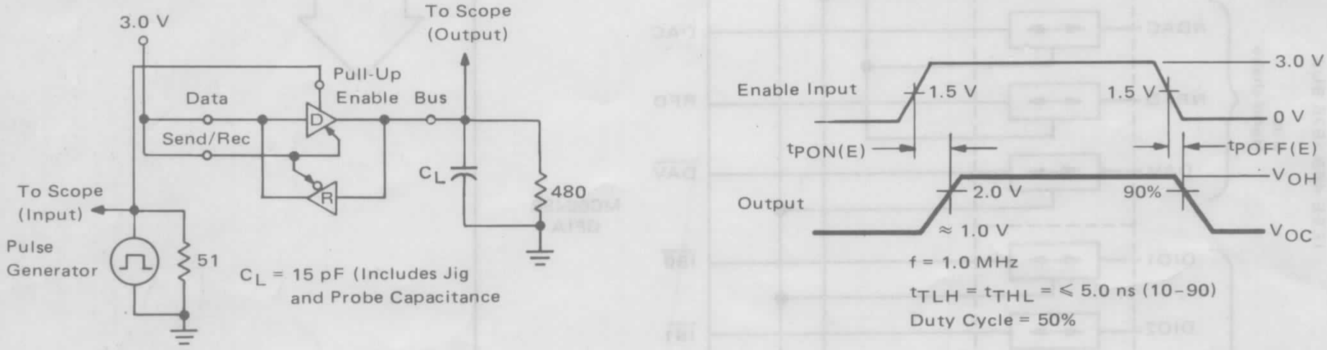


FIGURE 6 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

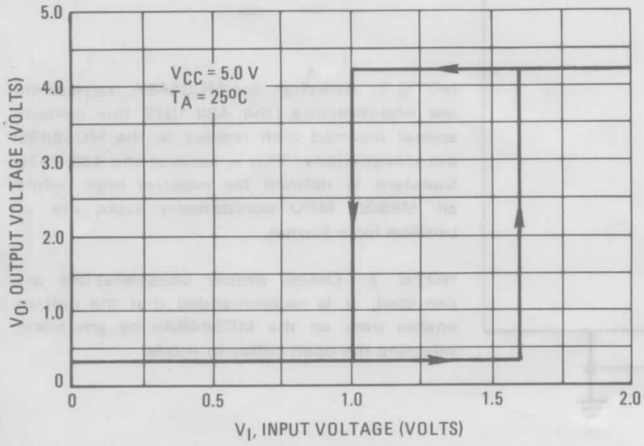
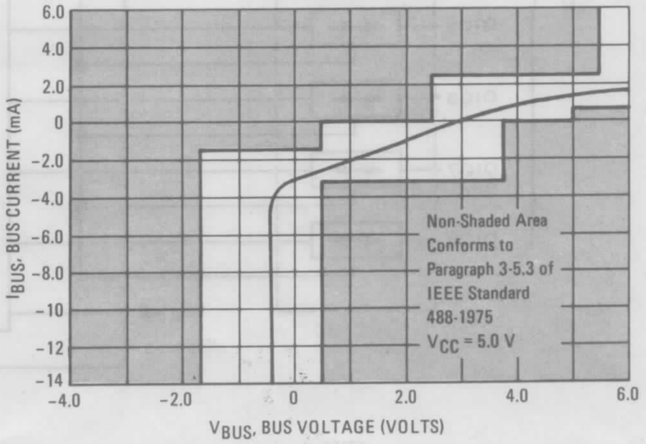
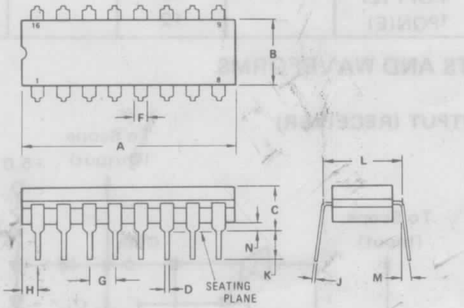


FIGURE 7 – TYPICAL BUS LOAD LINE



OUTLINE DIMENSIONS

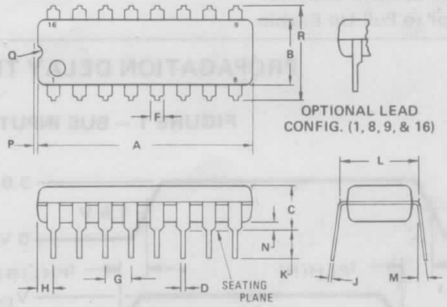


NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	3.18	0.30	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15^0	–	15^0
N	0.51	1.02	0.020	0.040

CASE 620-02

$R_{\theta JA} = 60^{\circ}C/W$ (Typical)



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. DIMENSION "R" TO BE MEASURED AT THE TOP OF THE LEADS (NOT AT THE TIPS).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	22.10	–	0.870
B	6.10	6.60	0.240	0.260
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	–	1.78	–	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	–	0.115	–
L	7.62 BSC		0.300 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	–	0.020	–
R	–	8.26	–	0.325

CASE 648-04

$R_{\theta JA} = 100^{\circ}C/W$ (Typical)

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

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SWITCHING CHARACTERISTICS (continued) (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Send/Receiver to Data					ns
Logic High to Third State	$t_{PHZ(R)}$	—	9.0	—	
Third State to Logic High	$t_{PZH(R)}$	—	17	—	
Logic Low to Third State	$t_{PLZ(R)}$	—	10	—	
Third State to Logic Low	$t_{PZL(R)}$	—	17	—	
Propagation Delay Time — Send/Receiver to Bus					ns
Logic High to Third State	$t_{PHZ(D)}$	—	12	—	
Third State to Logic High	$t_{PZH(D)}$	—	21	—	
Logic Low to Third State	$t_{PLZ(D)}$	—	11	—	
Third State to Logic Low	$t_{PZL(D)}$	—	19	—	
Turn-On Time — Enable to Bus					ns
Pull-Up Enable to Open Collector	$t_{POFF(E)}$	—	10	—	
Open Collector to Pull-Up Enable	$t_{PON(E)}$	—	12	—	

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

FIGURE 1 — BUS INPUT TO DATA OUTPUT (RECEIVER)

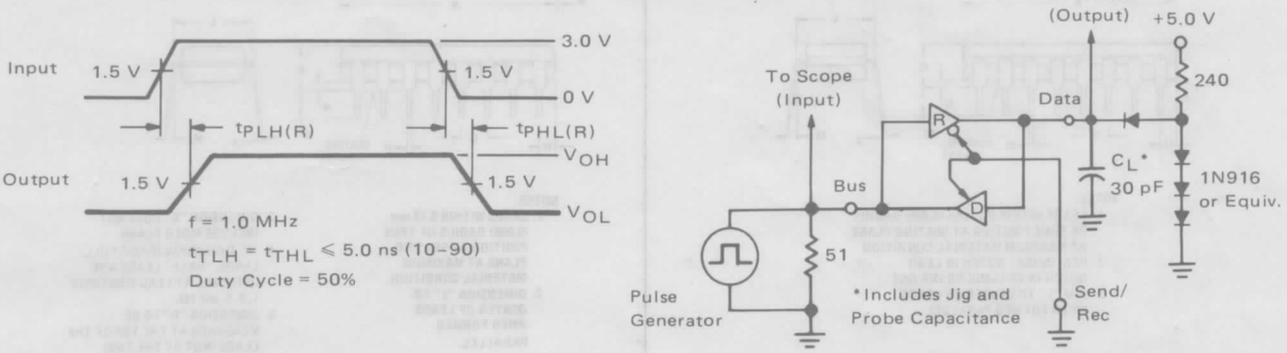

FIGURE 2 — DATA INPUT TO BUS OUTPUT (DRIVER)

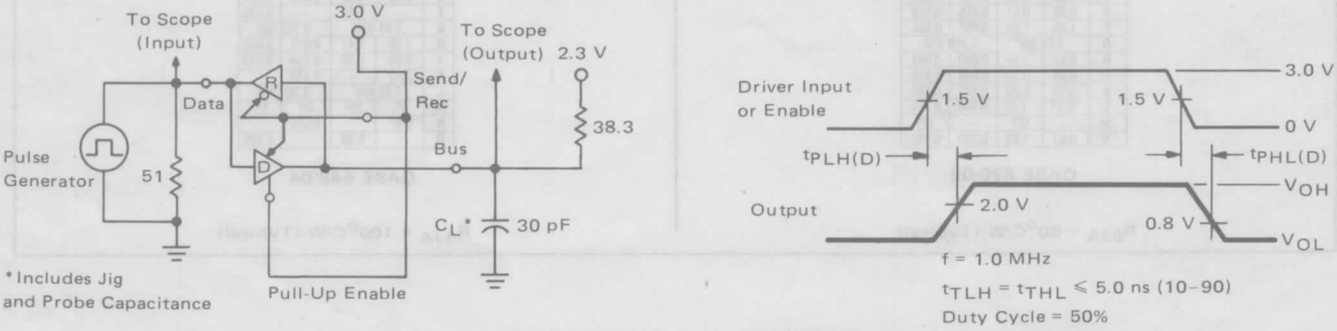

FIGURE 3 — SEND/RECEIVE INPUT TO BUS OUTPUT (DRIVER)